

FIG. 3a

ITEM	TERMI- NAL NO.	TERMI- NAL NAME	INPUT/ OUTPUT	FUNCTION
POWER SUPPLY	35,68	Vcc	—	+ 5V IS SUPPLIED.
	17,18 51,52	Vcc	—	GND IS CONNECTED.
OPERATION CONTROL SIGNAL	65	INCLK	INPUT	BASIC CLOCK OF MIVAC IS INPUTTED.
	66	TEST	INPUT	MIVAC OPERATION IS TESTED. SET THIS TERMINAL TO "LOW" LEVEL.
ACRTC INTERFACE SIGNAL	15	2CLK	OUTPUT	2CLK SIGNAL IS SUPPLIED TO ACRTC. THIS SIGNAL IS ASYMMETRIC, NAMELY, HAS DIFFERENT CYCLE LENGTHS IN THE FIRST HALF AND SECOND HALF OF A MEMORY CYCLE.
	14	MCYC	INPUT	MCYC SIGNAL FROM ACRTC IS INPUTTED. <del>MCYC</del> <del>MCYC</del> INDICATES "LOW" AND "HIGH" LEVELS WHEN ACRTC IS IN ADDRESS AND DATA CYCLES, RESPECTIVELY.
	12	<u>DRAW</u>	INPUT	<u>DRAW</u> SIGNAL FROM ACRTC IS INPUTTED. <u>DRAW</u> INDICATES WHETHER OR NOT ACRTC IS IN THE DRAW CYCLE. <u>DRAW</u> IS "LOW" LEVEL IN THE DRAW CYCLE AND IS "HIGH" LEVEL IN THE OTHER CYCLES.
	11	MRD	INPUT	MRD SIGNAL FROM ACRTC IS INPUTTED. MRD CONTROLS DATA TRANSFER DIRECTION BETWEEN FRAME BUFFER AND ACRTC. WHEN DATA IS READ FROM FRAME BUFFER, "HIGH" LEVEL IS INPUTTED. WHEN DATA IS WRITTEN IN FRAME BUFFER, "LOW" LEVEL IS INPUTTED.
	13	<u>AS</u>	INPUT	<u>AS</u> SIGNAL IS INPUTTED FROM ACRTC <u>AS</u> INDICATES PRESENCE OR ABSENCE OF MEMORY ACCESS.
	64	<u>HSYNC</u>	INPUT	<u>HSYNC</u> SIGNAL IS INPUTTED FROM ACRTC. UNDER CONDITIONS OF <u>HSYNC</u> ="LOW" AND <u>DRAW</u> ="HIGH", IF <u>AS</u> PULSE IS RECEIVED, <u>CS</u> BEFORE <u>RAS</u> REFRESH OPERATION IS CARRIED OUT.
	67	<u>VSNC</u>	INPUT	<u>VSNC</u> SIGNAL IS INPUTTED FROM ACRTC. RECEIVED <u>VSNC</u> IS DIVIDED BY TWO SO AS TO OUTPUTTED AS <u>VSNC</u> /2 SIGNAL AND IS ALSO USED TO CONTROL MULTIPLEXER OF VIDEO OUTPUT.
	2	<u>DISP 1</u>	INPUT	<u>DISP 1</u> SIGNAL IS INPUTTED FROM ACRTC. <u>DISP 1</u> INDICATES SCREEN DISPLAY PERIOD. ORDINARILY, SET "1" TO DISPLAY SIGNAL CONTROL (DSC) BIT OF ACRTC.
	1	<u>CUD 1</u>	INPUT	<u>CUD 1</u> SIGNAL IS INPUTTED FROM ACRTC. <u>CUD 1</u> IS LOADED WITH "LOW" LEVEL DURING GRAPHIC CURSOR DISPLAY PERIOD.
	6-10 16 19-28	MADO -MAD 15	INPUT/ OUTPUT	MODE-MAD 15 OF ACRTC ARE INPUTTED. THESE SIGNALS ARE USED AS FRAME BUFFER ACCESS ADDRESS IN ADDRESS CYCLE FOR MCYC="LOW", AS DATA INPUT/ OUTPUT FOR DATA TRANSFER BETWEEN ACRTC AND FRAME BUFFER IN DATA TRANSFER CYCLE FOR MCYC="HIGH".
	29-32	MA16- MA19	INPUT	FRAME BUFFER ACCESS ADDRESS MA16-MA19 IS INPUTTED FROM ACRTC.

FIG. 3b

ITEM	TERMI- NAL NO.	TERMI- NAL NAME	INPUT/ OUTPUT	FUNCTION
FRAME BUFFER INTERFACE SIGNAL	50	RAS	OUTPUT	RAS TIMING SIGNAL IS OUTPUTTED FOR DRAM.
	49	CS	OUTPUT	CS TIMING SIGNAL IS OUTPUTTED FOR DRAM.
	48	WE	OUTPUT	WE TIMING SIGNAL IS OUTPUTTED FOR DRAM.
	53	OE	OUTPUT	OE TIMING SIGNAL IS OUTPUTTED FOR DRAM.
	56,58 60,62 63,61 59,57 55,54	FA0 - FA 9	OUTPUT	MULTIPLEX ADDRESS IS OUTPUTTED FOR DRAM. ADDRESS TO BE MULTIPLEXED VARIES DEPENDING ON VCF 0 - VCF 3 AND VMD 0 ATTRIBUTE CODES.
	44,46 47,45 40,42 43,41	FD0 - FD 7	INPUT/ OUTPUT	FD IS 8-BIT INPUT/OUTPUT SIGNAL FOR DATA TRANSFER BETWEEN ACRTC AND FRAME BUFFER AND FOR FETCHING DISPLAY DATA READ FROM FRAME BUFFER. IN A CASE OF ONE MEMORY CHIP, FD 0 - FD 3 ARE USED, WHEREAS IN A CASE OF TWO FOUR MEMORY CHIPS, FD 0 - FD 7 ARE USED.
CRT DISPLAY INTERFACE SIGNAL	3	DOTCLK	OUTPUT	DOTCLK SIGNAL IS DELIVERED BY DIVIDING INCLK SIGNAL AS BASIC INPUT SIGNAL OF MIVAC BY 1, 2 AND 4. DIVISION RATIO IS SET DEPENDING ON VCF 0 - VCF 3 OF ATTRIBUTE CODE. OR
	33, 34 36, 37	VIDEO A -VIDEO D	OUTPUT	VIDEO A-D SIGNAL IS 4-BIT OUTPUT SIGNAL WHICH IS OBTAINED BY CONVERTING DISPLAY DATA FROM PARALLEL SIGNAL INTO SERIAL SIGNAL BY SHIFT REGISTER OF MIVAC AND WHICH IS DELIVERED DURING DISPLAY PERIOD INDICATED BY SHIF TEN OUTPUT. 4-BIT VIDEO SIGNAL IS DETERMINED BY ATTRIBUTE CODE SHIF TEN VCF 0 - VCF 3. SHIF TEN
	5	SHIF TEN SHIF TEN	OUTPUT	SHIF TEN INDICATES DISPLAY PERIOD OF VIDEO SIGNAL AND IS SET TO "HIGH" LEVEL DURING DISPLAY PERIOD. IN SINGLE ACCESS, DISP 1 FROM ACRTC IS ELONGATED BACKWARD BY ONE CYCLE, AND IN DUAL ACCESS, DISP 1 IS ELONGATED BACKWARD BY TWO CYCLES SO AS TO PRODUCE THIS SIGNAL.
	4	VSYNC/2	OUTPUT	VSYNC/2 SIGNAL IS INPUTTED TO ACRTC. VSYNC IS DIVIDED BY TWO FOR PRODUCING THIS SIGNAL.
OTHERS	38	BL2IRQ	OUTPUT	BL 2IRQ IS SET BY BLINK 2 (MA 19) INPUTTED IN ATTRIBUTE CYCLE. DURING ATTRIBUTE CYCLE, WHEN BLINK 2 IS AT "HIGH" LEVEL, BLINK 2 IS SET TO "LOW" LEVEL. BL 2IRQ
	39	IRQCLR	INPUT	IRQCLR SIGNAL IS USED TO CLEAR BL 2IRQ SIGNAL. WHEN "LOW" IS INPUTTED TO IRQCLR, BL 2IRQ IS CLEARED TO "HIGH" LEVEL.

FIG. 4

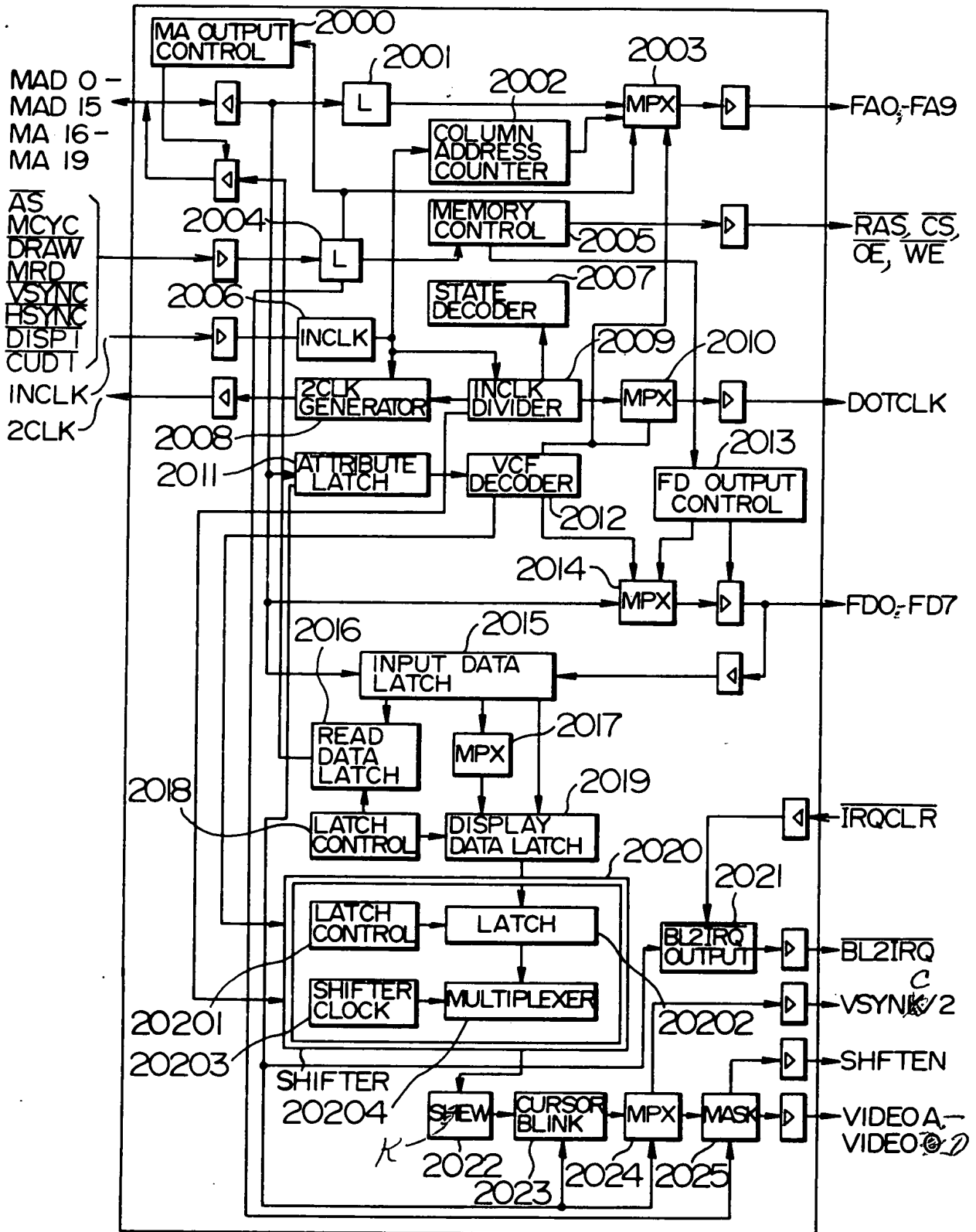


FIG. 7

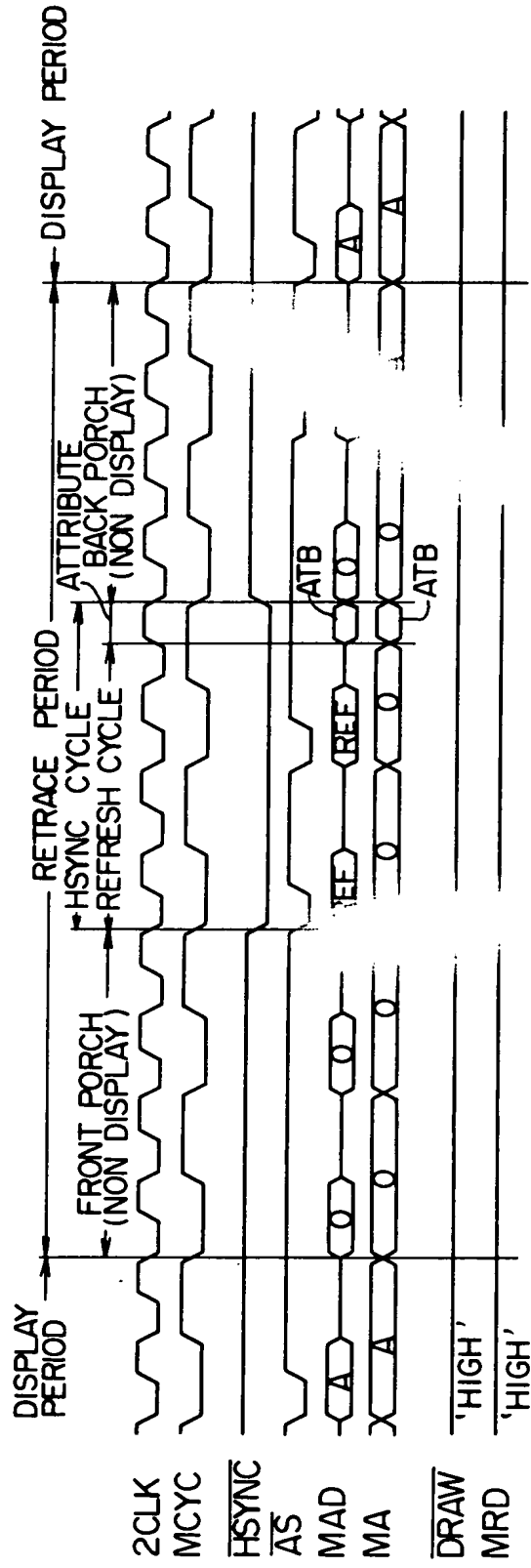
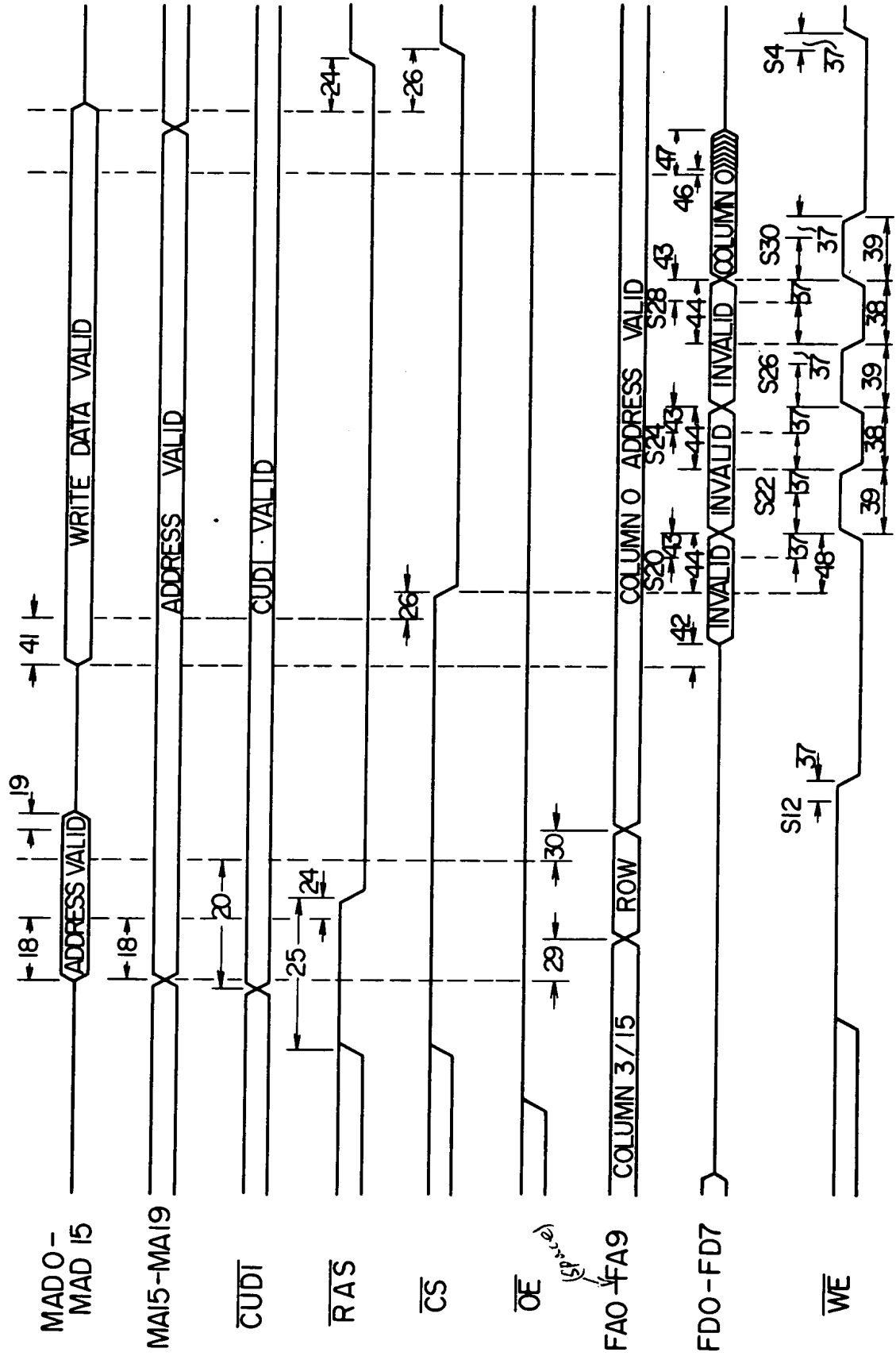


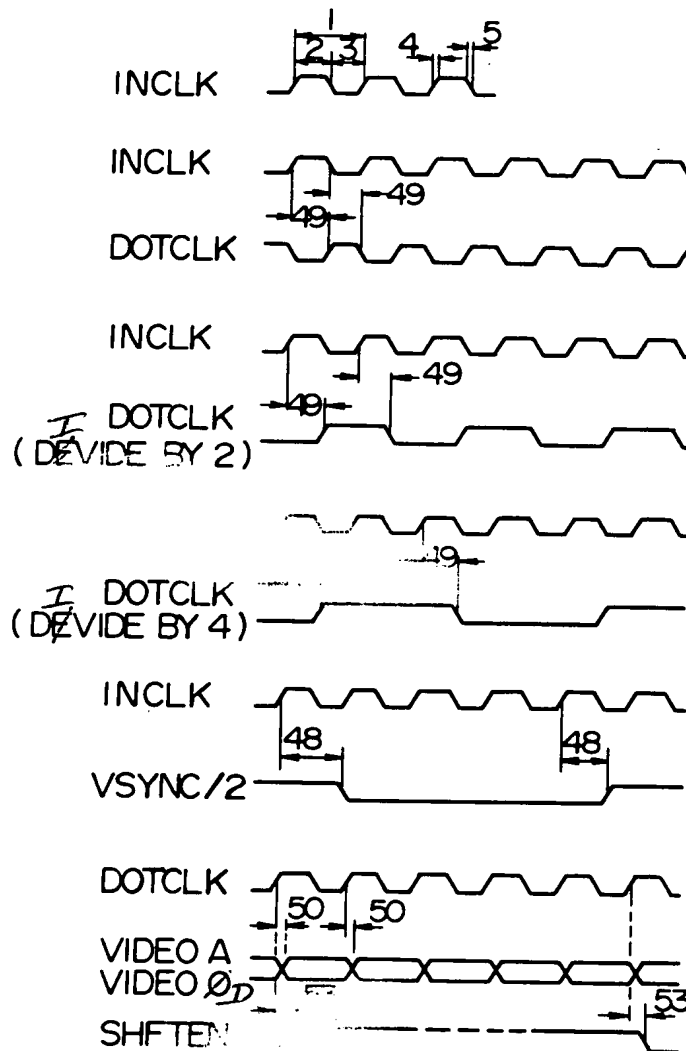
FIG. 11

CUR I	CUR O	CURSOR DISPLAY COLOR
0	0	BLACK ( VIDEO A - VIDEO D = 0 )
0	1	WHITE ( VIDEO A - VIDEO D = 1 )
1	0	COLOR REVERSION FOR EACH BIT OF VIDEO A - VIDEO D <sup>(i p a c e)</sup>
1	1	COLOR REVERSION FOR EACH BIT OF VIDEO A - VIDEO D (VIDEO D IS KEPT UNCHANGED)

FIG. 20b



F I G. 25



F I G. 26

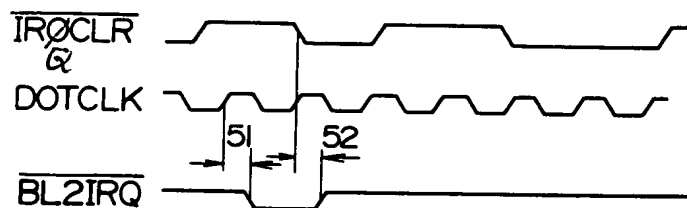
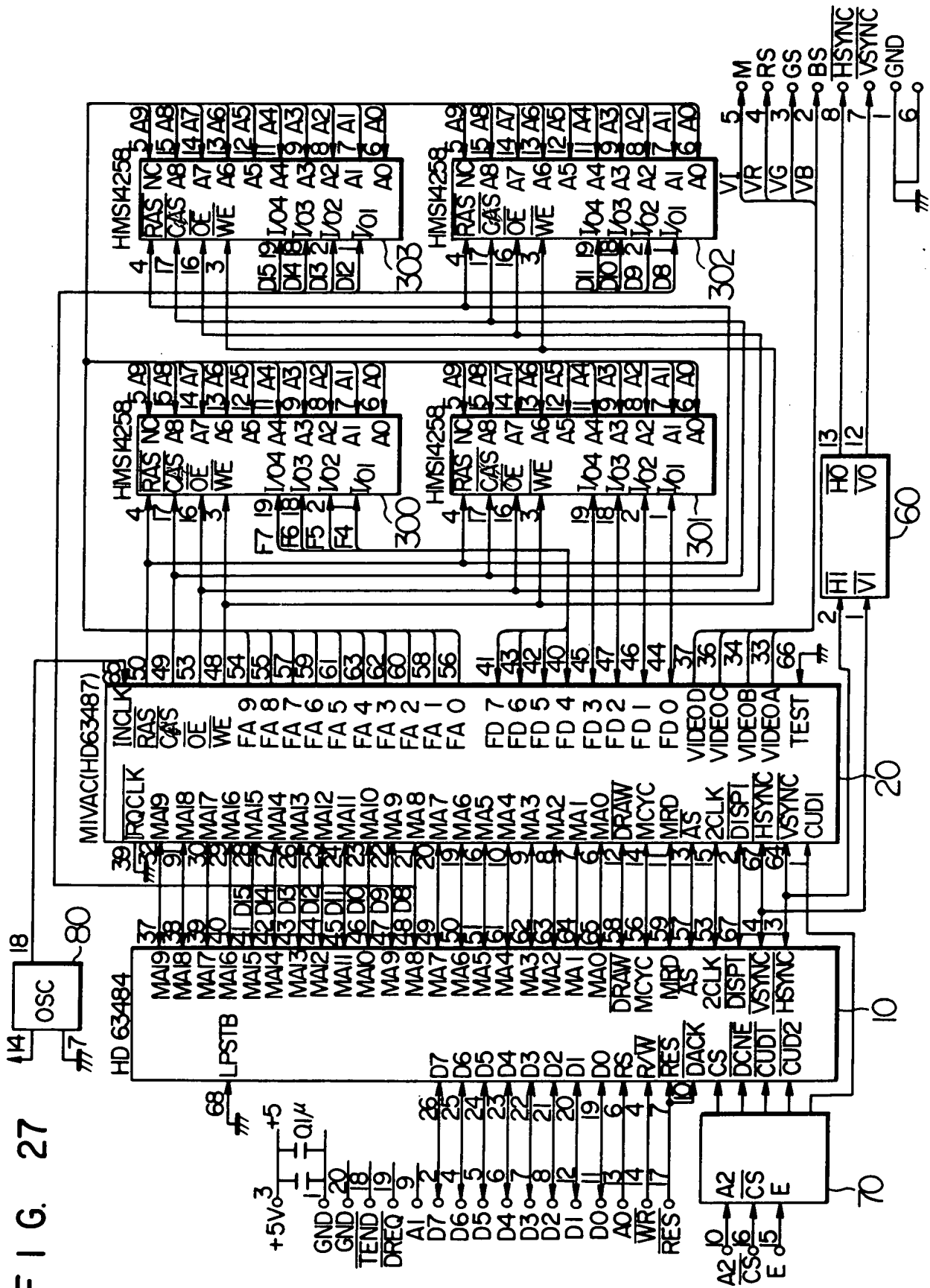
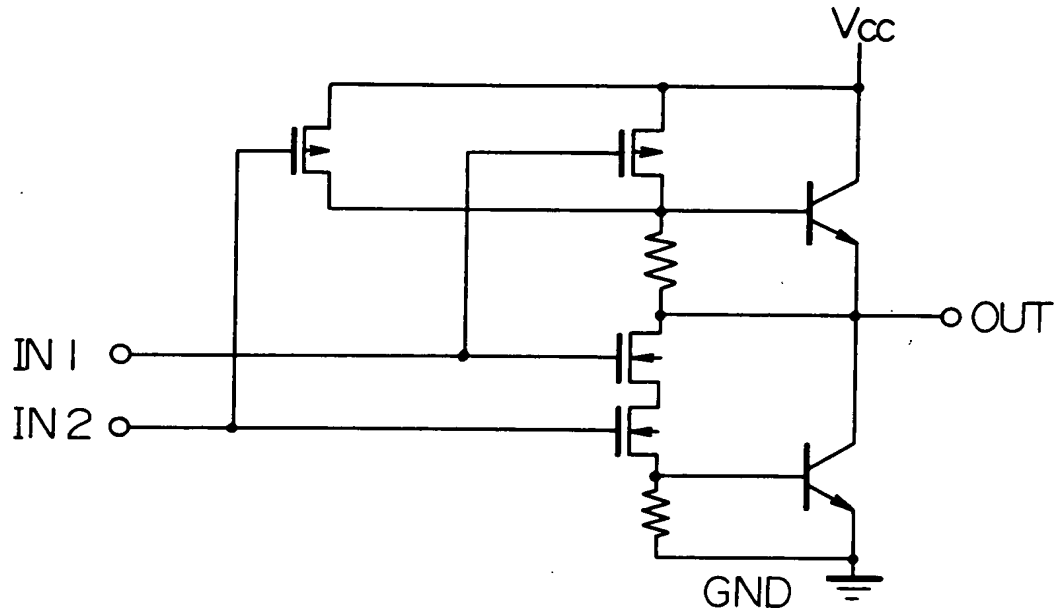


FIG. 27



F I G. 28



F I G. 29a

FA	4 ACCESSSES / MCYC ( DRAW , DISPLAY )				16 ACCESSSES / 2 MCYCS ( DISPLAY )			
	256Kx4-BIT ( VMDO=0 )		1M x 4-BIT ( VMDO=1 )		256Kx 4-BIT ( VMDO=0 )		1M x 4-BIT ( VMDO=1 )	
	ROM <sub>W</sub>	COLUMN	ROM <sub>W</sub>	COLUMN	ROM <sub>W</sub>	COLUMN	ROM <sub>W</sub>	COLUMN
9	—	—	MAD 8	NC0	—	—	MAD 8	NC0
8	MAD 9	NC1	MAD 9	NC1	MAD 9	NC1	MAD 9	NC1
7	MAD 8	NC2	MA 17	MAD 7	MAD 8	NC2	MA 17	MAD 7
6	MAD 7	MAD 6	MA 16	MAD 6	MAD 7	MAD 6	MA 16	MAD 6
5	MAD 15	MAD 5	MAD 15	MAD 5	MAD 15	MAD 5	MAD 15	MAD 5
4	MAD 14	MAD 4	MAD 14	MAD 4	MAD 14	MAD 4	MAD 14	MAD 4
3	MAD 13	MAD 3	MAD 13	MAD 3	MAD 13	MAD 3	MAD 13	MAD 3
2	MAD 12	MAD 2	MAD 12	MAD 2	MAD 12	MAD 2	MAD 12	MAD 2
1	MAD 11	MAD 1	MAD 11	MAD 1	MAD 11	WC1	MAD 11	WC1
0	MAD 10	MAD 0	MAD 10	MAD 0	MAD 10	WC0	MAD 10	WC0

[ ] : COLUMN ADDRESS COUNTER